CLAIMS

1. A method of testing an electronic memory device comprising:

loading test data and/or instructions into a control logic circuit portion associated with a matrix array of memory cells and storage circuitry using a test operation control device, temporarily, for said control logic, said test operation control device being external of, and temporarily connected to, said memory device.

2. A method according to claim 1, wherein said test operation control device comprises a matrix cell array external to the memory device.

3. A method according to claim 1, wherein said test operation control device comprises a control logic external to the memory device.

4. A method according to claim 1, characterized in that said temporary connection is established through data pins and address pins of the memory device, as well as over respective connecting buses.

5. A method according to claim 1, wherein said control logic is incorporated in a non-volatile memory device.

6. A control device for testing electronic memory devices having provided with a matrix array of memory cells and a control logic circuit portion associated with the memory cell array, as well as with circuitry associated with said control logic, comprising a memory unit external of and detachably connected to the memory device.

7. A device according to claim 6, wherein the detachable connection is established through data pins and address pins of the memory device.

8. A device according to claim 6, wherein said external memory unit is a non-volatile type.

9. A device comprising:

an internal memory array integrated onto a semiconductor substrate;

a control logic circuit integrated onto the semiconductor substrate; and

a test control device, external to the semiconductor substrate, having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array.

10. The device of claim 9, wherein the test control device includes a circuit for simulating the control logic circuit, detachably connected to the semiconductor substrate.

11. The device of claim 10, wherein the circuit for simulating the internal memory array and the circuit for simulating the control logic circuit are integrated into one test device.

12. The device of claim 9, wherein the circuit for simulating the internal memory array is an external memory array.

13. The device of claim 9, wherein the circuit for simulating the internal memory array comprises a software program in an external memory executed by a testing circuit.

14. A method for testing a memory array integrated, with a control logic circuit, onto a semiconductor substrate, comprising:

simulating the control logic circuit, using an external connected circuit;

performing test operations with the memory array and the external connected circuit; and

observing interactions between the memory array and the external connected circuit.

15
~~14.~~ A method for testing a control logic circuit integrated, with a memory array, onto a semiconductor substrate, comprising:

simulating the memory array, using an external connected circuit;

performing test operations with the control logic circuit and the external connected circuit; and

observing interactions between the control logic circuit and the external connected circuit.